SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY
Khairatabad, Hyderabad
(An Autonomous Institution)
M.TECH. - VLSI SYSTEM DESIGN
EFFECTIVE FROM ACADEMIC YEAR 2023-24 ADMITTED BATCH
R23 COURSE STRUCTURE AND SYLLABUS

I YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
5857AB	Digital System Design with FPGAs	3	0	0	3
5857AA	CMOS Analog IC Design	3	0	0	3
5857AE 5857AC 5857AD	1. Pattern Recognition and Machine Learning 2. CMOS Mixed Signal Design 3. Memory Technologies	3	0	0	3
5857AG 5857AF 5857AH	1. Communication Buses & Interfaces 2. ARM Microcontrollers 3. Embedded Real Time Operating System	3	0	0	3
585702	Digital System Design with FPGAs Lab	0	0	4	2
585701	CMOS Analog IC Design Lab	0	0	4	2
5857AJ	Research Methodology & IPR	2	0	0	2
Audit – I	Audit Course – I	2	0	0	0
	Total Credits	**16**	**0**	8	**18**

I YEAR II – SEMESTER

Course Code	Course Title	L	T	P	Credits
5857AV	VLSI Advanced Physical Design	3	0	0	3
5857AW	System Verilog Test Benches using UVM	3	0	0	3
5857AX 5857AY 5857AZ	1. IoT Architectures and System Design 2. SoC Design 3. Design for Testability	3	0	0	3
5857BA 5857BB 5857BC	1. Device Modeling 2. RF IC Design 3. Hardware and Software Co-Design	3	0	0	3
585703	VLSI Advanced Physical Design Lab	0	0	4	2
585704	System Verilog Test Benches using UVM Lab	0	0	4	2
585705	Mini Project with Seminar	0	0	4	2
Audit – II	Audit Course- II	2	0	0	0
	Total Credits	**14**	**0**	**12**	**18**

Audit Course I & II:

1. 5857AN - English for Research Paper Writing
2. 5857AM - Disaster Management
3. 5857AR - Sanskrit for Technical Knowledge
4. 5857AU - Value Education
5. 5857AK - Constitution of India
6. 5857AP - Pedagogy Studies
7. 5857AT - Stress Management by Yoga
8. 5857AQ - Personality Development Through Life Enlightenment Skills

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
5857AB - DIGITAL SYSTEM DESIGN WITH FPGAs (PC – I)

Pre-Requisite: Switching Theory and Logic Design

Course Objectives:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an overview of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

Course Outcomes:

1. To exposes the design approaches using FPGAs.
2. To provide in depth understanding of Fault models.
3. To understands test pattern generation techniques for fault detection.
4. To design fault diagnosis in sequential circuits.
5. To provide understanding in the design of flow using case studies.

UNIT- I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB and slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]

UNIT- II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models forsequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design strategies for multi-clock sequential circuits. [TEXTBOOK-2]

UNIT- III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT- IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.
Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT - V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.3]

TEXT BOOKS:

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C.LEE,PHI, 2008.

REFERENCE BOOKS:

1. Logic Design Theory- N.N.Biswas, PHI.
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.
3. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR- I SEMESTER
VLSI SYSTEM DESIGN
5857AA - CMOS ANALOG IC DESIGN (PC - II)

Pre-requisite: Analog Electronics

Course Objectives: Analog circuits play a very crucial role in all electronic systems and due to continued miniaturization; many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes: After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT - I
MOS Devices and Modeling
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small- Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT- II
Analog CMOS Sub-Circuits
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors- Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror,Current and Voltage References, Band gap Reference.

UNIT – III
CMOS Amplifiers
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT - IV
CMOS Operational Amplifiers
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT - V
Comparators
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
5857AE - PATTERN RECOGNITION AND MACHINE LEARNING (PE – I)

Prerequisite: Statistics and Linear Algebra

Course Objectives:

1. The student will be able to understand the mathematical formulation of patterns.
2. To study the various linear models.
3. Understand the basic classifiers.
4. Can able to distinguish different models.

Course Outcomes: On completion of this course student will be able to

1. Familiar the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Use the different kernel methods.
4. Design the Markov and Mixed models.

UNIT-I

Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

UNIT-II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

UNIT-III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines-RVM for regression, Analysis of sparsity,RVM for classification

UNIT-IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields - Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in generalgraphs, Loopy belief propagation, Learning the graph structure.

UNIT-V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM- Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

TEXT BOOKS:

1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press,volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006.

REFERENCE BOOKS:

1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.
2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
5857AC - CMOS MIXED SIGNAL DESIGN (PE-I)

Pre-Requisites: Analog Electronics

Course Objectives: The objectives of this course are to

1. Introduce circuit design concepts for basic building blocks used in mixed-signal integratedcircuit designs.
2. Provide students with the skills to design mixed-signal integrated circuits with these buildingblocks.
3. Understand design and operation of basic analog circuits.
4. Know mixed signal circuits like DAC, ADC, PLL etc.
5. Design and analysis of switched capacitor circuits
6. Analysis basic data conversion algorithms and circuits.

Course Outcomes: After completing this course, each student will have demonstrated proficiency in:

1. Designing CMOS analog circuits to achieve performance specifications.
2. Analyzing CMOS based switched capacitor circuits.
3. Designing data converters and know how to use these in specific applications
4. Design mixed-signal circuits with understanding design flow.

UNIT- I
Switched Capacitor Circuits
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT- II
Phased Lock Loop (PLL)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities,Jitter in PLLs, Delay locked loops, applications

UNIT - III
Data Converter Fundamentals
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT- IV
Nyquist Rate A/D Converters
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT - V
Oversampling Converters
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

TEXT BOOKS

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002.

2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013.

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
5857AD - MEMORY TECHNOLOGIES (PE – 1)

Course Objectives:

1. To know the RAM technologies, architecture and applications
2. To know the circuit design concepts of Non-volatile memories
3. To understand the Memory package density technologies.

Course Outcomes: At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Know, how of the state-of-the-art memory chip design

UNIT- I

Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT- II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design andArchitecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

UNIT- III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT- IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-Access Memories (MRAMs), Experimental Memory Devices.

UNIT- V

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXT BOOKS:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
2. Kiyoo Itoh, "VLSI memory chip design", Springer International Ed.

REFERENCE BOOKS:

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
5857AG - COMMUNICATION BUSES AND INTERFACES (PE – II)

Course Objectives:

1. To know how to select the suitable Buses for different applications
2. To know the architecture of CAN and applications
3. To understand the use of PCIe, USB etc.,
4. To know the serial communication protocol

Course Outcomes: At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT - I

Serial Busses - Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I2C, SPI

UNIT - II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT - III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT - IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT - V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

TEXT BOOKS:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references on www.can-cia.org, http://www.pcisig.com/, www.pcisig.com, http://www.usb.org/, www.usb.org

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
5857AF - ARM MICROCONTROLLERS (PE - II)

Course Objectives:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes: After completing this course the student will be able to:

1. Explore the selection criteria of ARM processors by understanding the functional level trade offissues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M.

UNIT - I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT - II

Introduction to the Arm Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple- Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT - III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT - IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly languagesyntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4- specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT - V

Floating Point Operations About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- overview,FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP

on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter,Fast Fourier

transform, FIR filter.

TEXT BOOKS:

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, ElsevierPublications, 3rd Ed.,

REFERENCE BOOKS:

1. Arm System on Chip Architectures – Steve Furber, Edison Wesley, 2000.
2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
5857AH - EMBEDDED REAL TIME OPERATING SYSTEMS (PE – II)

Prerequisite: Computer Organization and Operating System

Course Objectives: The objectives of this course are:

1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes: Students will:

1. Be able to explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
2. Able describe how a real-time operating system kernel is implemented.
3. Explain how the real-time operating system implements time management.
4. Be able to work with real time operating systems like RT Linux, Vx Works, MicroC /OS-II, TinyOS

UNIT - I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

.

UNIT - III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOK:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, TMH, 2007.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH-IYEAR-I SEMESTER
VLSI SYSTEM DESIGN
585702 - DESIGN DIGITAL SYSTEM DESIGN WITH FPGAs LAB (Lab – I)

Part –I:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using encoder (without and with parity).
5. Design of Combinational circuit using multiplexer.
6. Design of 4 bit binary to gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, comparator in all 3 styles.
8. Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequencecounter
10. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial outand Parallel in Parallel Out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier, Divider.
13. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
14. Implementing the above designs on FPGA kits.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN
585701 - CMOS ANALOG IC DESIGN LAB (Lab – II)

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Design analog Circuit using CMOS.
2. Use EDA tools like Cadence, Mentor Graphics and other open source software tools likeNgspice

List of Experiments:

1) Use V_{DD} = 1.8V for 0.18 um CMOS process, V_{DD} = 1.3V for 0.13 um CMOS Process and V_{DD} = 1Vfor 0.09 um CMOS Process.
   a) Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS.
   b) Plot I_D vs. V_{GS} at particular drain voltage (low) for NMOS, PMOS and determine V_t.
   c) Plot log I_D vs. V_{GS} at particular gate voltage (high) for NMOS, PMOS and determine I_{OFF} andsub-threshold slope.
   d) Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e) Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use V_{DS} = 30 mVTo extract V_{th} use the following procedure.
      i. Plot gm vs V_{GS} using NGSPICE and obtain peak gm point.
      ii. Plot y= I_D/(gm)1/2 as a function of V_{GS} using Ngspice.
      iii. Use Ngspice to plot tangent line passing through peak gm point in y (V_{GS}) plane anddetermine V_{th}.
   f) Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.

   Tabulate your result according to technologies and comment on it.

2) Use V_{DD} = 1.8V for 0.18 um CMOS process, V_{DD} =1.2V for 0.13 um CMOS Process and V_{DD} = 1Vfor 0.09 um CMOS Process.
   a) Perform the following
      i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine transitionvoltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying V_{DD}.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL,tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload =50 fF)
   c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use C_{in}= 0.012 pF, C_{load} = 4pF, R_{load} = k)

3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18 um and 0.13 umtechnology and compare its frequencies and time period.

4) Perform the following

a) Draw small signal voltage gain of the minimum-size inverter in 0.18 um and 0.13 um technology as a function of input DC voltage. Determine the small signal voltage gain at theswitching point using Ngspice and compare the values for 0.18 um and 0.13 um process.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18 um technology. (W/L) MN=5, (W/L) MP=10 and L= 0.5 um for both transistors.

i. Establish a test bench, as explained in the lecture, to achieve $V_{DSQ} = V_{DD}/2$.

ii. Calculate input bias voltage if bias current = 50 uA.

iii. Use Ngspice and obtain the bias current. Compare its value with 50 uA.

iv. Determine small signal voltage gain, - 3 dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive timeconstant of the output and compare it with the time constant resulted from -3dB BW

vi. Use Ngspice to determine input voltage range of the amplifier

5) Three OP-AMP INA. V_{dd} = 1.8V V_{ss} = 0V, CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OP-AMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.

ii. Draw the schematic of INA.

iii. Obtain parameters of the op-amp macro model such that

a. low-frequency voltage gain =5 x 104,
b. unity gain BW (fu) =500 KHz,
c. input capacitance = 0.2 pF,
d. output resistance =,
e. CMRR=120 dB

iv. Draw schematic diagram of CMRR simulation setup.

v. Simulate CMRR of INA using AC analysis (it's expected to be around 6 dB below CMRRof OP-AMP).

vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch ineach resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

vii. Repeat (iii) to (vi) by considering CMRR of all OP-AMPs to be 90 dB.

6) Technology: UMC 0.18 um, V_{DD}=1.8V. Use MAGIC or Microwind.

a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.

b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.

c) Use extracted netlist and obtain tPHL, tPLH for the middle inverter using Eldo.

d) Use interconnect length obtained and connect the second and third inverter.

Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delaytimes with corresponding values obtained in part ‘c’

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - I SEMESTER
VLSI SYSTEM DESIGN

5857AJ - RESEARCH METHODOLOGY AND IPR

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to:

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work andinvestment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT - I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.

Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT - II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT - III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT - IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science &engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - II SEMESTER

VLSI SYSTEM DESIGN

5857AV - VLSI ADVANCED PHYSICAL DESIGN (PC - III)

Course Objectives:

1. To know the IR drop, Power requirements, power mesh design, and electro migration.
2. To know the design of power optimization techniques.
3. To understand the On-chip variations and their impact on performance of design.
4. To know Foundry design rules and implementation methodologies.

Course Outcomes: Student will be able to:

1. Design power mesh for given specifications, analyze IR drop and EM issues and fix them.
2. Implement the low power intent of the design using current industry standard UPF.
3. Verify whether the design meets the power intent in UPF
4. Perform physical verification both at LVS & DRC level and fix all issues.

UNIT - I

Power Analysis: Introduction to power analysis, Goals and objectives, Data preparation, Power meshdesign, Static IR analysis, Dynamic IR analysis, Signal and power EM.

UNIT - II

Low Power Design – I: Introduction, Low power optimization in the SOC flow, Special cells for powermanagement, Architectural techniques for low power.

UNIT - III

Low Power Design – II: Low power implementation techniques (multi voltage, power gating etc.), UPFformats, Low power checks.

UNIT - IV

Advanced STA: Hierarchical STA (ILM, XILM, ETM), On-chip variations, Advanced on-chip variations, Parametric on chip variations, Introduction to LVF.

UNIT - V

Physical Verification: Physical verification - Introduction, goals and objectives, design rule check, layout versus schematic check and electrical rule check, Design for manufacturability - Introduction, DFM aware routing, DFM checks and fixing (pattern matching, MAS).

TEXT BOOK:

1. Rakesh Chadha and J. Bhasker, "An ASIC Low Power Primer", Springer, 2013.

REFERENCE BOOKS:

1. Voltus Reference Manuals, 17.12.000.
2. Tempus Reference Manual, 17.12.000.
3. Calibre Reference Manual, 2017.1_17.12

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH.- I YEAR- II SEMESTER
VLSI SYSTEM DESIGN
5857AW - SYSTEM VERILOG TEST BENCHES USING UVM (PC - IV)

Course Objectives:

1. To Learn System Verilog for Verification constructs.
2. To understand the UVM methodology.
3. To know UVM implementation for Verilog RTLs.

Course Outcomes: Students will be able to:

1. Implement test bench programs using system Verilog.
2. Develop random stimulus and SVAs using system Verilog.
3. Develop a UVM test bench with all its features.

UNIT – I

Verification Basics: Introduction, Verification need, Test bench components, Directed versus random stimulus, Code coverage versus functional coverage, Types of code coverage, Verification plan and test plan.

UNIT - II

System Verilog – I: Introduction, Constructs, Interface and object-oriented programming concepts.

UNIT – III

System Verilog – II: Randomization, Functional coverage and system verilog assertions.

UNIT – IV

UVM Test Bench Architecture: Introduction, UVM components and UVM phases.

UNIT – V

UVM Methodology: UVM component configuration and factory, Modelling UVM transactions, UVM sequence, Virtual sequencer, Component communication and UVM reporting.

TEXT BOOKS:

1. Janic Bergeron, "Writing Testbenches: Functional Verification of HDL Models", 2nd Ed., Kluwer Academic Publishers, 2003.
2. Stuart Sutherland, Simon Davidmann and Peter Flake, "System Verilog for Design", 2nd Ed., Springer, 2006.

REFERENCE BOOK:

1. Reference Verification Methodology User Guide, Version 8.5.11 – Synopsis

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - II SEMESTER
VLSI SYSTEM DESIGN

5857AX - IOT ARCHITECTURES AND SYSTEM DESIGN (PE - III)

Course Objectives

1. To Know the definition and basic concepts of IoT
2. Learn the interfacing the IoT and M2M
3. To understand the Architecture of IoT

Course Outcomes: Students will be able to:

1. Integrate the sensors and actuator depending on the applications
2. Interface the IoT and M2M with value chains
3. Write Python programming for Arduino, Raspberry Pi devices
4. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.,

UNIT - I

IoT introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT - II

IoT and M2M: M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

UNIT - III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT - IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack, IoT data management and compute stack

UNIT - V

IoT System design: Challenges associated with IoT, Emerging pillors of IoT, Agricultural IoT, Vehicular IoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. Sudip Misra, Anandarup Mukherjee, Arijit Roy "Introduction to IOT", Cambridge UniversityPress.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry "IoT Fundamentals Networking technologies, protocols, and use cases for IoT", Cisco Press

REFERENCE BOOKS:

1. Cuno pfister, "Getting started with the internet of things", O Reilly Media, 2011
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to ConnectingEverything", 1 st Edition, Apress Publications.
3. "Internet of Things concepts and applications", Wiley
4. Arshdeep Bahga,Vijay Madisetti "Internet of Things A Hands on approach", Universities Press

5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, "Internet of things" John Wileyand Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/MakerMedia Publishers.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR- II SEMESTER
VLSI SYSTEM DESIGN
5857AY - SOC DESIGN (PE - III)

Course Objectives:

1. To learn ASIC design concepts and strategies
2. To know the NISC applications and advantages
3. To familiar with simulation and synthesis process

Course Outcomes: At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches
2. Design SoC based system for engineering applications
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

UNIT - I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT - II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilationand synthesis of embedded processors.

UNIT - III

Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT - IV

Low power SoC design / Digital system Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT - V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report, analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

REFERENCE BOOKS

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - II SEMESTER
VLSI SYSTEM DESIGN
5857AZ - DESIGN FOR TESTABILITY (PE - III)

Pre-Requisite: Digital System Design

Course Objectives:

1. To acquire the knowledge of fundamental concepts of testing
2. To provide broad understanding the fault simulation.
3. To illustrate the framework of Built-in-self test and Boundary scan methods.

Course Outcomes: Students will be able to

1. Acquire verification knowledge and test evaluation
2. Design for testability rules and techniques.
3. Utilize the scan architectures for different digital circuits.
4. Acquire the knowledge of design of built-in-self test.

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSITechnology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations ofScan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, "Essential of Electronic Testing for Digital, Memory and MixedSignal VLSI Circuits", Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design", Jaico Publishing House.
2. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR - II SEMESTER
VLSI SYSTEM DESIGN
5857BA - DEVICE MODELLING (PE - IV)

Course Objectives:

1. To obtain the functional relationship among the terminal electrical variables of the device thatis to be modeled
2. To know the physical properties of materials and devices
3. To know the MOS transistor low frequency model
4. To understand the characteristics of the FinFETs and its applications

Course Outcomes: Students will be able to

1. Develop a functional relationship among the terminal electrical variables of the device that is to be modeled.
2. Describe the behavior of all components successfully
3. Perform the simulation and analyze the VLSI circuits
4. Use the FinFET for various applications

UNIT - I

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Mid gap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.

UNIT - II

MOS Capacitor Characteristics and Non idealities: CV characteristics of MOS, LFCV and HFCV, Non- idealities in MOS, oxide fixed charges, interfacial charges.

UNIT - III

The MOS transistor: Small signal modeling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

UNIT - IV

The bipolar transistor: Eber's-Moll model; charge control model; small-signal models for low and highfrequency and switching characteristics.

UNIT - V

FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

TEXT BOOKS:

1. S. M. Sze, "Physics of Semiconductor Devices", 2nd Ed., Wiley Eastern, 1981.
2. Y. P. Tsividis, "Operation and Modelling of the MOS Transistor", McGraw-Hill, 1987.
3. E. Takeda, "Hot-carrier Effects in MOS Transistors", Academic Press, 1995.
4. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer. 2009

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH.- I YEAR- II SEMESTER
VLSI SYSTEM DESIGN
5857BB - RF IC DESIGN (PE- IV)

Pre-requisites: NIL.

Course Objectives:

1. To learn the concepts of RF frequency analysis and component modelling.
2. To give understanding of various types of RF filter circuits.
3. To familiarize the Concept of RF amplifiers and oscillators.

Course Outcomes: Upon completing this course, the student will be able to

1. Analyze the behavior of high frequency components.
2. Calculate the scattering parameters of various RF components and analyze the various filterparameters.
3. Implement component modelling and biasing networks.
4. Design the various RF filters, amplifiers, oscillators and mixers.

UNIT - I

Introduction: Importance of RF design dimensions and units frequency spectrum RF behavior of passive components, high frequency resistors, high frequency capacitors, high frequency inductor, chip components and circuit board Considerations chip resistors chip capacitors and surface mount inductors.

UNIT - II

RF filter design: Scattering parameters: definition, meaning chain, scattering matrix, conversion between S- and Z-parameters, signal flow chart modeling, generalization basic resonator and filter configurations: low pass, high pass, band pass and band stop type filters-filter implementation using unit element and kuroda's identities transformations-coupled filters

UNIT - III

Active RF component modeling: RF diode models: nonlinear and linear models transistor models: large signal and small signal BJT models, large signal and small signal FET models-scattering parameters device characterization.

Matching and biasing networks: Impedance Matching using discrete components: Two component matching networks, Forbiddenregions, frequency response and quality factor, T and PI matching networks-amplifier classes of operation and biasing networks: classes of operation and efficiency of amplifiers, biasing networks for BJT, biasing networks for FET.

UNIT - IV

RF transistor amplifier design: Characteristics of amplifier-amplifier power relations RF sources, transducers power gain, additional power relations-stability consideration: stability circles, unconditional stability and stabilization methods-unilateral and bilateral design for constant gain noise figure circles-constant VSWR circles.

UNIT - V

RF oscillators and mixers: Basic oscillator models: Negative resistance oscillator, feedback oscillatordesign, design steps, quads oscillators- fixed frequency, high frequency oscillator- basic characteristics of mixers: concepts, frequency domain considerations, single ended mixer design, single and double balanced mixers.

TEXT BOOKS:

1. RF circuit design- theory and applications - Reinhold Ludwig Pavel bsetchko- Pearson education India 2000
2. Radio frequency and microwave communication circuits- analysis and design- devendrak Mishra- wiley student edition- john wiley and sons inc

REFERENCE BOOKS:

1. Radio frequency and microwave electronics mathew m rarmaneah PEI
2. RF circuit design christoper BOWIK Cheryl aijuni and john butler Elsevier science 2008
3. Secrets of RF circuit design joseph jcarr TMH 2000
4. Design of RF and microwave amplifiers and oscillators peter lD
5. Madison a brief artech house 2000.
6. The design of CMOS radio frequency integrated circuits thomas h Lee 2/e Cambridge University Press 2004.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR- II SEMESTER
VLSI SYSTEM DESIGN
5857BC - HARDWARE AND SOFTWARE CO-DESIGN (PE - IV)

Course Objectives:

1. To know the Co-design Issues, prototype and emulation techniques
2. To learn Architecture specific techniques
3. To know the different tool for design

Course Outcomes: Students will be able to:

1. Acquire the knowledge on various models of Co-design.
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools during Co-design.
4. Implement validation methods and adaptability.

UNIT - I

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT- II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulationenvironments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051- Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi- language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf –Springer, 2009.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer AcademicPublishers, 2002.

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer,2010

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR- II SEMESTER
VLSI DESIGN

585703 - VLSI ADVANCED PHYSICAL DESIGN LABORATORY (Lab-III)

Note:

i. Minimum 10 experiments have to be conducted.
ii. All experiments are to be done using say Voltus (for IR), say Conformal LP (low power checks) and say Caliber (for physical verification).
iii. Modifications can be made to the list based on contemporary Industry requirements.
iv. EDA tools can be changed based on availability and requirements.

List of Experiments:

1. Run power analysis and report dynamic and static power numbers from Innovus.Study howthe power is changing with different activity factors.
2. Run Static IR analysis using Voltus and generate and understand the IR map.
3. Run Dynamic IR analysis using Voltus and generate and understand the Dynamic IR map.
4. Write UPF and load into the Tool.
5. Implement power gating on a design using Innovus.
6. Add Isolation cells in the design using Innovus and based on UPF.
7. Run CLP and make sure power intent is satisfied on the post power gated design.
8. Run timing analysis on the design. Understand various sections in the timing report.
9. Generate ETM of the design
10. Run cross talk delay analysis and understand the cross talk impact on the critical path.
11. Run timing analysis by enabling OCV and study the impact of OCV on the timing.
12. DRC
13. LVS

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD

(AN AUTONOMOUS INSTITUTION)

M.TECH. - I YEAR- II SEMESTER
VLSI SYSTEM DESIGN

585704 - SYSTEM VERILOG TEST BENCH USING UVM LABORATORY (Lab-IV)

Note:

i. Minimum 10 experiments have to be conducted.

ii. Experiments are covering three components of any standard verification environment - Testsidentification, system Verilog constructs, assertions, stimulus generation and application using randomization techniques, functional coverage, developing UVC, creating tests and running simulations.

iii. All experiments are to be done using NCVERILOG and ICC (for coverage).

iv. Modifications can be made to the list based on contemporary Industry requirements.

List of Experiments:

1. Constrained random stimulus generation.
2. Functional coverage.
3. System Verilog assertions.
4. Interface.
5. Test plan development.
6. UVM environment and test cases flow.
7. UVM transaction item and sequences.
8. UVM driver and monitor.
9. UVM agent creation.
10. UVM scoreboard.
11. UVM environment and basic test development.
12. Create test cases as per test plan.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AN - ENGLISH FOR RESEARCH PAPER WRITING (Audit Course - I & II)

Prerequisite: None

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT- I:
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT- II:
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT- III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT- IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills areneeded when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT- V:
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York DordrechtHeidelberg London, 2011

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AM - DISASTER MANAGEMENT (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance inspecific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches,
- Planning and programming in different countries, particularly their home country or the countriesthey work in

UNIT- I

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT- II

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT- III

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT- IV

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT- V

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall ofIndia, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep & DeepPublication Pvt. Ltd., New Delhi.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AR - SANSKRIT FOR TECHNICAL KNOWLEDGE (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancingthe memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledgefrom ancient literature

Course Outcomes: Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

UNIT-I:
Alphabets in Sanskrit,

UNIT-II:
Past/Present/Future Tense, Simple Sentences

UNIT-III:
Order, Introduction of roots,

UNIT-IV:
Technical information about Sanskrit Literature

UNIT-V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/ REFERENCES:

1. "Abhyaspustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya SanskritSansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AU - VALUE EDUCATION (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

UNIT-I:
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration.Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:
Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science ofreincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford UniversityPress, New Delhi

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AR - CONSTITUTION OF INDIA (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in theearly years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrivalof Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working),
Philosophy of the Indian Constitution: Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AP - PEDAGOGY STUDIES (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy makingundertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms indeveloping countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions,and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT-I:

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:

Professional development: alignment with classroom practices and follow-up support, Peer support,Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:

Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31(2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY, KHAIRATABAD, HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AT - STRESS MANAGEMENT BY YOGA (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To achieve overall health of body and mind
- To overcome stress

Course Outcomes: Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT-I:
Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:
Yam and Niyam.

UNIT-III:
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:
Asan and Pranayam

UNIT-V:
i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

SHADAN WOMEN'S COLLEGE OF ENGINEERING & TECHNOLOGY KHAIRATABAD HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH. (VLSI SYSTEM DESIGN)
5857AQ - PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes: Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality andachieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.