SHADAN WOMEN'S COLLEGE OF ENGINEERING AND TECHNOLOGY, KHAIRATABAD, HYDERABAD
(An Autonomous Institution)
M.TECH. IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS
EFFECTIVE FROM ACADEMIC YEAR 2023-24 ADMITTED BATCH

R23 COURSE STRUCTURE AND SYLLABUS

I YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
5806AA	ARM Microcontrollers	3	0	0	3
5806AB	Digital Systems Design with FPGAs	3	0	0	3
5806AC 5806AD 5806AE	1. Pattern Recognition and Machine Learning 2. TCP/IP and ATM Networks 3. VLSI Technology and Design	3	0	0	3
5806AF 5806AG 5806AH	1. CMOS Analog IC Design 2. Communication Buses & Interface 3. Embedded Real Time Operating Systems	3	0	0	3
5806AJ	Research Methodology & IPR	2	0	0	2
580601	ARM Microcontrollers Lab	0	0	4	2
580602	Digital Systems Design with FPGAs Lab	0	0	4	2
Audit - I	Audit Course – I	2	0	0	0
	Total	**16**	**0**	8	**18**

I YEAR II – SEMESTER

Course Code	Course Title	L	T	P	Credits
5806AV	Advanced Computer Architecture	3	0	0	3
5806AW	Embedded System Design	3	0	0	3
5806AX 5806AY 5806AZ	1. IoT Architecture and system Design 2. Design of Fault Tolerant Systems 3. VLSI Signal Processing	3	0	0	3
5806BA 5806BB 5806BC	1. SoC Design 2. Hardware and Software co-design 3. Ad-hoc and Wireless Sensor Networks	3	0	0	3
580603	Embedded Systems Lab	0	0	4	2
580604	Simulation Lab	0	0	4	2
580605	Mini Project with Seminar	0	0	4	2
Audit - II	Audit Course – II	2	0	0	0
	Total	**14**	**0**	**12**	**18**

Audit Course I & II:

1. 5806AK - Constitution of India
2. 5806AM - Disaster Management
3. 5806AN - English for Research Paper Writing
4. 5806AP - Pedagogy Studies
5. 5806AQ - Personality Development Through Life Enlightenment Skills
6. 5806AR - Sanskrit for Technical Knowledge
7. 5806AT - Stress Management by Yoga
8. 5806AU - Value Education

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M.TECH. - I YEAR - I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AA - ARM MICROCONTROLLERS (PC - I)

Prerequisite: Microprocessors and Microcontrollers

Course Objectives:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes: After completing this course the student will be able to:

1. Explore the selection criteria of ARM processors by understanding the functional level trade offissues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M.

UNIT -I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT -II

Introduction to the Arm Instruction Set : Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple- Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT -III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT -IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4- specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT -V

Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXT BOOKS:

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Arm System on Chip Architectures – Steve Furber, Edison Wesley, 2000.
2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AB - DIGITAL SYSTEM DESIGN WITH FPGAs (PC – II)

Pre-Requisite: Switching Theory and Logic Design

Course Objectives:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an overview of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

Course Outcomes:

1. To exposes the design approaches using FPGAs.
2. To provide in depth understanding of Fault models.
3. To understands test pattern generation techniques for fault detection.
4. To design fault diagnosis in sequential circuits.
5. To provide understanding in the design of flow using case studies.

UNIT-I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB andslice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]

UNIT-II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design stratagies for multi-clock sequential circuits. [TEXTBOOK-2]

UNIT-III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronozation, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT-IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT -V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.3]

TEXT BOOKS:

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C.LEE,PHI, 2008.

REFERENCE BOOKS:

1. Logic Design Theory-N.N.Biswas,PHI.
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.
3. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AC -PATTERN RECOGNITION AND MACHINE LEARNING (PE – I)

Prerequisite: Statistics and Linear Algebra

Course Objectives:

1. The student will be able to understand the mathematical formulation of patterns.
2. To study the various linear models.
3. Understand the basic classifiers.
4. Can able to distinguish different models.

Course Outcomes: On completion of this course student will be able to

1. Familiar the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Use the different kernel methods.
4. Design the Markov and Mixed models.

UNIT -I

Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

UNIT -II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

UNIT -III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplaceapproximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity,RVM for classification

UNIT -IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

UNIT -V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM- Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesianlinear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

TEXT BOOKS:

1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press, volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006.

REFERENCE BOOKS:

1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd 2001.
2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009.

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AD - TCP/IP AND ATM NETWORKS (PE - I)

Pre-requisite: Computer Networks

Course Objectives: The main objectives of the course are:

1. To study Network Layer Protocols, Next Generation IP protocols
2. To learn about User Datagram Protocol, Transmission Control Protocol and stream control Transmission protocol.
3. To understand techniques to improve QoS
4. To learn about Transport Layer Protocols for Ad Hoc Wireless Networks .
5. To study the features of ATM networks and various Interconnection Networks

Course Outcomes: At the end of the course, the student will be able to:

1. Get the concept of Network Layer Protocols and Transport Layer Protocols.
2. Understand and analyze about UDP, TCP AND SCTP protocols, flow and error controltechniques.
3. Learn congestion control mechanisms and techniques to improve Quality of Service inswitched networks
4. To understand the performance of TCP in Ad-hoc networks and various modified versions ofTCP in ad-hoc networks
5. To understand features of Virtual circuit networks like ATM networks and their applications Design and analyze various types of Inter connection Networks.

UNIT -I

Network Layer: Network Layer Services**,** Packet switching**,** , Network Layer Performance, IPv4 Addresses, Internet protocol(IP), ICMP v4, IPv6 Addressing, IPv6 protocol, ICMPv6 protocol, Transition from IPv4to IPv6,Mobile IP

Forwarding of IP Packets, Delivery- Direct Versus Indirect Delivery, Forwarding- Forwarding Techniques, Forwarding Process, Routing Table, Unicast routing- Routing algorithms, Unicast routing protocols, Multicast routing, Multicasting basics.

UNIT -II

Transport Layer Introduction to Transport Layer, Transport layer services, Connectionless Versus Connection Oriented Protocols, Transport Layer Protocols: Simple Protocols, Stop and Wait Protocols,Go Back N Protocol, Selective Repeat Protocol, Bidirectional Protocols: Piggybacking Transport layer protocols Services and Port Numbers.

UDP, TCP and SCTP

User Datagram Protocol (UDP): User Datagram, UDP Services, UDP Applications

Transmission Control Protocol (TCP): TCP Services, TCP Features, Segments, TCP Connection, State Transition Diagram, Windows in TCP, Flow and Error Control, TCP Timers,

SCTP: SCTP Services, SCTP Features, Packet Format, An SCTP Association SCTP Flow and ErrorControl

UNIT -III

Traditional TCP: Congestion Control, Additive Increase Multiplicative Decrease (AIMD), Slow Start, Fast recovery, fast retransmit

TCP in Wireless Domain: Traditional TCP, TCP over wireless**,** Snoop TCP, TCP-Unaware Link Layer Indirect TCP, Mobile TCP, Explicit Loss Notification, WTCP, TCP SACK , Transaction-Oriented TCP

Transport Layer Protocols for Ad Hoc Wireless Networks: TCP Over Ad Hoc Wireless Networks- Feedback-Based TCP, TCP with Explicit Link Failure Notification, TCP-Bus, Ad Hoc TCP, Split TCP.

UNIT -IV

Congestion Control and Quality of Service: Quality of Service- Flow Characteristics, Flow Classes, Techniques to Improve QoS- Scheduling, Traffic Shaping, Resource Reservation, Admission Control,Integrated Services- Signaling, Flow Specification, Admission, Service Classes, RSVP, Problems withIntegrated Services , Differentiated Services.

Queue Management: Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

UNIT -V

ATM Networks: ATM-Design Goals, Problems, Architecture, Switching, ATM Layers

SONET/SDH: Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks

Interconnection Networks: Introduction, Banyan Networks, Properties, Crossbar switch, Three stage Class Networks, Rearrangeable Networks, Folding algorithm, Benes Networks, Lopping algorithm, Bit allocation algorithm.

TEXT BOOKS:

1. Data Communications and Networking - B. A.Forouzan, 5th edition, TMH, 2013.
2. Mobile Communications by Jochen H. Schiller, 2nd Edition, Pearson-Wesley, 2003.
3. Ad Hoc Wireless networks: Architectures and Protocols- C. Siva Ram Murthy and B. S.Manoj, PHI, 2004

REFERENCE BOOKS:

1. ATM Fundamentals –N.N Biswas, Adventure Books,1998
2. Data Communications and Computer Networks - Prakash C. Gupta, PHI, 2006.
3. Data and Computer Communications - William Stallings, 8th ed., PHI, 2007.

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AE -VLSI TECHNOLOGY AND DESIGN (PE – I)

Pre-requisite: Switching Theory And Logic Design

Course Objectives:

1. Students from other engineering background to get familiarize with large scale integration technology.
2. To expose fabrication methods, layout and design rules.
3. Learn methods to improve Digital VLSI system's performance.
4. To know about VLSI Design constraints.
5. Visualize CMOS Digital Chip Design.

Course Outcomes: Students will be able to:

1. Review of FET fundamentals for VLSI design.
2. Acquires knowledge about stick diagrams and layouts.
3. Design the subsystems based on VLSI concepts.
4. Do the Floorplanning and Routing for VLSI systems.

UNIT-I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids — Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT -II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT -III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT -IV

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT -V

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRCPress, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AF - CMOS ANALOG ICDESIGN (PE – II)

Pre-Requisite: Analog Electronics

Course Objectives: Analog circuits play a very crucial role in all electronic systems and due tocontinued iniaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in theMOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes: After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT -I
MOS Devices and Modeling:
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV
CMOS Operational Amplifiers:
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AG - COMMUNICATION BUSES AND INTERFACES (PE - II)

Course Objectives:

1. To known how to select the suitable Buses for different applications
2. To known the architecture of CAN and applications
3. To understand the use of PCIe, USB etc.,
4. To known the serial communication protocol

Course Outcomes: At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT -I

Serial Busses- Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I^2C, SPI

UNIT -II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT -III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT -IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT -V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

TEXT BOOKS:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
2. Jan Axelson, "USB Complete", PenramPublications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", MindsharePress

REFERENCE BOOKS:

1. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition,2005.
2. Serial Front Panel Draft Standard VITA 17.1 –200x
3. Technical references on www.can-cia.org, http://www.pcisig.com/ www.pcisig.com, http://www.usb.org/ www.usb.org

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AH - EMBEDDED REAL TIME OPERATING SYSTEMS (PE – II)

Prerequisite: Computer Organization and Operating System

Course Objectives: The objectives of this course are:

1. To provide broad understanding of the requirements of Real Time Operating Systems.
2. To make the student understand, applications of these Real Time features using case studies.

Course Outcomes: Students will be:

- Able to explain real-time concepts such as preemptive multitasking, task priorities, priority inversions, mutual exclusion, context switching, and synchronization, interrupt latency and response time, and semaphores.
- Able to describe how a real-time operating system kernel is implemented.
- Able to Explain how the real-time operating system implements time management.
- Able to work with real time operating systems like RT Linux, Vx Works, MicroC /OS-II,Tiny OS

UNIT -I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT -II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

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UNIT -III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT -IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT -V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOK:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal,TMH, 2007.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

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DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AJ - RESEARCH METHODOLOGY AND IPR

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT- I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.

Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT- II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT- III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT- IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT- V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

SHADAN WOMEN'S COLLEGE OF ENGINEERING AND TECHNOLOGY KHAIRATABAD HYDERABAD
(AN AUTONOMOUS INSTITUTION)
M.TECH.- I YEAR- I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
580601 - ARM MICROCONTROLLERS LAB (Lab – I)

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 development boards.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED onceevery five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGBLED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

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M.TECH. - I YEAR - I SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
580602 - DIGITAL SYSTEM DESIGN WITH FPGAs LAB (Lab – II)

Part -I:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

List of Assignments:

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using encoder (without and with parity).
5. Design of Combinational circuit using multiplexer.
6. Design of 4 bit binary to gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, comparator in all 3 styles.
8. Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequencecounter
10. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel inSerial out and Parallel in Parallel Out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier, Divider.
13. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
14. Implementing the above designs on FPGA kits.

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AV - ADVANCED COMPUTER ARCHITECTURE (PC – III)

Course Objectives:

1. To understand the fundamental of computer design
2. To know the pipelines and parallelism concepts
3. To know the issues in interconnect networks

Course Outcomes: At the end of the course, students will be able to:

1. Familiarize the instruction set , memory addressing of Computer
2. Handle the issues in pipelining and parallelism
3. Familiarize the practical issues in inter network

UNIT -I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT -II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT -IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared — memory architecture, Synchronization.

UNIT -V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", Mc Graw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AW - EMBEDDED SYSTEM DESIGN (PC – IV)

Pre-Requisite: Microprocessor and Microcontrollers

Course Objectives

1. To differentiate between a General purpose and an Embedded System.
2. To provide knowledge on the building blocks of Embedded System.
3. To understand the requirement of embedded firmware and its role in API.

Course Outcomes

1. Expected to differentiate the design requirements between General Purpose and EmbeddedSystems.
2. Expected to acquire the knowledge of firmware design principles.
3. Expected to understand the role of Real Time Operating System in Embedded Design.
4. To acquire the knowledge and experience of task level Communication in any EmbeddedSystem.

UNIT- I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT- II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT- III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT- IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization
Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOK:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AX - IOT ARCHITECTURES AND SYSTEM DESIGN (PE – III)

Course Objectives:

1. To Know the definition and basic concepts of IoT
2. Learn the interfacing the IoT and M2M
3. To understand the Architecture of IoT

Course Outcomes: Students will be able to

1. Integrate the sensors and actuator depending on the applications
2. Interface the IoT and M2M with value chains
3. Write Python programming for Arduino, Raspberry Pi devices
4. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.,

UNIT -I

IoT introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT,IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT -II

IoT and M2M: M2M to IoT — A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

UNIT -III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT -IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack ,IoT data management and compute stack

UNIT -V

IoT System design: Challenges associated with IoT, Emerging pillors of IoT, Agricultural IoT, VehicularIoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. Sudip Misra, Anandarup Mukherjee,Arijit Roy "Introduction to IOT", Cambridge Univ. Press.
2. David Hanes,Gonzalo salgueiro,Patrick Grossetete,Rob barton,Jerome henry "IoTFundamentals Networking technologies,protocols,and usecases for IoT",Cisco Press

REFERENCE BOOKS:

1. Cuno pfister, "Getting started with the internet of things", O Reilly Media,2011
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1 st Edition, Apress Publications.
3. "Internet of Things concepts and applications",Wiley
4. Arshdeep Bahga,Vijay Madisetti "Internet of Things A Hands on approach",UniversitiesPress
5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, "Internet of things" JohnWiley and Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/Maker Media Publishers.

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AY - DESIGN OF FAULT TOLERANT SYSTEMS (PE – III)

Pre-Requisite: Digital System Design

Course Objectives:

1. To acquire the knowledge of fundamental concepts in fault tolerant design.
2. To provide broad understanding of fault diagnosis and tolerant design approach.
3. To illustrate the framework of test pattern generation using semi and full automatic approach.

Course Outcomes: Students will be able to

1. Acquire Design knowledge of requirements of self-check-in circuits and LFSR.
2. Knowledge of design for testability rules and techniques for combinational circuits.
3. Utilize the scan architectures for different digital circuits.
4. Acquire the knowledge of design of built-in-self test.

UNIT -I

Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT -II

Self Checking circuits &Fail safe Design: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

Fail Safe Design- Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT -III

Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrometestable designs.

Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique-Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT -IV

Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designinga BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self-test(BEST), Random Test socket (RTS), LSSD On-chip self-test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT -V

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS,Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXT BOOKS:

1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala,PHI, 1984.
2. Digital System Test and Testable Design using HDL models and Architectures -ZainalabedinNavabi, Springer International Ed.,

REFERENCE BOOKS:

1. Digital Systems Testing and Testable Design-MironAbramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books
2. Essentials of Electronic Testing- Bushnell &VishwaniD.Agarwal,Springers.
3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806AZ - VLSI SIGNAL PROCESSING (PE- III)

Course Objectives:

1. To learn pipling and parallel processing concepts for low power designs
2. To known the folding and unfolding architecture properties and advantages
3. To understand the systolic architectures and their applications
4. To known the significance of fast convolution.

Course Outcomes: On successful completion of the module, students will be able to:

- Modify the existing or new DSP architectures suitable for VLSI.
- Use folding and unfolding algorithms and applications.
- Implement fast convolution algorithms.
- Design processors for signal processing and wireless applications with low power concepts.

UNIT -I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms
Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power
Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT -II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems
Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V

Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches
Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, Wiley Inter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall,1985.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing – Medisetti V. K, IEEE Press (NY), 1995.

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806BA - SOC DESIGN (PE – IV)

Course Objectives:

1. To learn ASIC design concepts and strategies
2. To known the NISC applications and advantages
3. To familiar with simulation and synthesis process

Course Outcomes: At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches
2. Design SoC based system for engineering applications
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby inclinetowards entrepreneurship & skill development.

UNIT -I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP)concepts.

UNIT -II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT -III

Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT -IV

Low power SoC design / Digital system Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT -V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press,2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

REFERENCE BOOKS:

1. RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann,2008
3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806BB - HARDWARE AND SOFTWARE CO-DESIGN (PE – IV)

Course Objectives:

1. To Known the Co-design Issues, prototype and emulation techniques
2. To learn Architecture specific techniques
3. To known the different tool for design

Course Outcomes: Students will be able to:

1. Acquire the knowledge on various models of Co-design.
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools during Co-design.
4. Implement validation methods and adaptability.

UNIT - I

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051- Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi- language co-simulation, the cosyma system and lycos system.

TEXT BOOK:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.

REFERENCE BOOKS:

1. Hardware / Software Co- Design - Giovanni De Micheli, MariagiovannaSami,Kluwer Academic Publishers, 2002.
2. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer,2010

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(AN AUTONOMOUS INSTITUTION)
M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
5806BC - AD-HOC AND WIRELESS SENSOR NETWORKS (PE- IV)

Prerequisite: Wireless Sensor Networks

Course Objectives: The objectives of this course are to make the student

1. To study the fundamentals of wireless Ad-Hoc Networks.
2. To study the operation and performance of various Adhoc wireless network protocols.
3. To study the architecture and protocols of Wireless sensor networks.

Course Outcomes: On completion of this course student will be able to:

1. Design performance based MAC layer protocols of Adhoc wireless networks.
2. Design performance based routing protocol of Adhoc wireless network.
3. Design performance based transport layer protocol of Adhoc wireless networks.
4. Distinguish between protocols used in Adhoc wireless network and wireless sensor networks.

UNIT - I

Wireless LANs and PANs: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.

AD HOC WIRELESS NETWORKS: Introduction, Issues in Ad Hoc Wireless Networks.

UNIT - II

MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT - III

Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT – IV

Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj,2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - JagannathanSarangapani, CRC Press.

REFERENCE BOOKS:

1. Ad-Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh , 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

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580603 - EMBEDDED SYSTEMS LAB (LAB – III)

List of Experiments:

1. **Functional Testing Of Devices**
   Flashing the OS on to the device into a stable functional state by porting desktop environment withnecessary packages.
2. **Exporting Display On To Other Systems**
   Making use of available laptop/desktop displays as a display for the device using SSH client & X11display server.
3. **GPIO Programming**
   Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430**
   Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity**
   Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator**
   Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3Vbattery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V).
7. **Dice Game Simulation**
   Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface**
   Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Open wrt To the Device**
   Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board**
    Building and hosting a simple website (static/dynamic) on the device and make it accessible online.There is a need to install server (eg: Apache) and thereby host the website.
11. **Webcam Server**
    Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission**
    Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz).

Note : Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

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M.TECH. - I YEAR - II SEMESTER
DIGITAL SYSTEMS & COMPUTER ELECTRONICS
580604 - SIMULATION LAB (LAB – IV)

List of Experiments Using gem5/ equivalent:

1. Introduction to GEM5/equivalent simulator. Features on a variety of CISC and RISCprocessors.
2. Introduction to ESESC/equivalent simulator. Features on a variety of Processors
3. Do a comprehensive search to list out all possible Computer Architecture Simulators.
4. Creation of ISA -ALPHA machine and Simulating
5. Code Scheduling using a Program – Prime Number Determination -MIPS instruction set
6. Implementation of Atomic Simple CPU - Conventional MIPS with five stage pipelining
7. Implementation of Timing Simple CPU - Conventional MIPS with five stage pipelining
8. Implementation of Inorder CPU - Minor with seven stage pipelining
9. Implementation of out-of-order CPU - Minor with seven stage pipelining
10. Implementation of Classic Memory model using L1 & L2 Cache
11. Creation of Unicore CPU for Multiprogrammed Benchmark – SPEC CPU 2006 as per thefollowing specifications:
    L1 Cache -16KB Associativity – 2- Way; L2 Cache Size : 256 KB Associativity -8-way

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(AN AUTONOMOUS INSTITUTION)
M.TECH. (DSCE)
5806AN - ENGLISH FOR RESEARCH PAPER WRITING (Audit Course - I & II)

Prerequisite: None

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT- I:
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT- II:
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT- III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT- IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills areneeded when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT- V:
skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York DordrechtHeidelberg London, 2011

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M.TECH. (DSCE)
5806AM -DISASTER MANAGEMENT (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- critically evaluate disaster risk reduction and humanitarian response policy and practice frommultiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance inspecific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countriesthey work in

UNIT- I

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT- II

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills,Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT- III

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports:Governmental and Community Preparedness.

UNIT- IV

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT- V

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

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M.TECH. (DSCE)
5806AR -SANSKRIT FOR TECHNICAL KNOWLEDGE (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes: Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

UNIT-I:
Alphabets in Sanskrit,

UNIT-II:
Past/Present/Future Tense, Simple Sentences

UNIT-III:
Order, Introduction of roots,

UNIT-IV:
Technical information about Sanskrit Literature

UNIT-V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/ REFERENCES:

1. "Abhyaspustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya SanskritSansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

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M.TECH. (DSCE)
5806AU -VALUE EDUCATION (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

UNIT-I:
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:
Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:
Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:
Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:
Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford UniversityPress, New Delhi

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5806AK - CONSTITUTION OF INDIA (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working),
Philosophy of the Indian Constitution: Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:
Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role.Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:
Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

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M.TECH. (DSCE)
5806AP -PEDAGOGY STUDIES (Audit Course - I & II)

Prerequisite: None

Course Objectives: Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions,and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT-I:

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:

Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31(2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher educationresearch project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

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M.TECH. (DSCE)
5806AT -STRESS MANAGEMENT BY YOGA (Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To achieve overall health of body and mind
- To overcome stress

Course Outcomes: Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT-I:
Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:
Yam and Niyam.

UNIT-III:
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:
Asan and Pranayam

UNIT-V:
i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama(Publication Department), Kolkata

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M.TECH. (DSCE)
5806AQ -PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course - I & II)

Prerequisite: None

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes: Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality andachieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya SanskritSansthanam, New Delhi.